REMARKS

The Examiner is thanked for the thorough examination and search of the subject. The applicants respectfully request continued examination of the above-indicated application as per 37 CFR 1.114.

Claims 281-373 are pending, wherein claims 281-286 are currently amended, claims 287-370 are newly added, and claims 1-280 are canceled.

Response to Claim Rejections under 35 U.S.C. 102 and 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 281 and 287-300

As currently amended, independent claim 281 is recited below:

281. A method for fabricating a circuit component, comprising:

joining a preformed die and a preformed substrate;

after said joining said preformed die and said preformed substrate, depositing a circuit layer comprising a first portion over said preformed die and a second portion over said preformed substrate but not over said preformed die; and

depositing a gold bump over said circuit layer.

Section I

Reconsideration of Claim 281 rejected under 35 U.S.C. 102(b) as being anticipated by Sakurai (US6,078,104) is requested based on the following remarks.

In merit to meet requirement of patentability, Applicants have amended Claim 281 with the limitation that "after said joining said preformed die and said preformed

substrate, depositing a circuit layer comprising a first portion over said preformed die and a second portion over said preformed substrate but not over said preformed die".

Applicants respectfully assert that the method claimed in claim 281 patentably distinguishes over the citations by Sakurai (US6,078,104).

Sakurai teaches that a method for fabricating a circuit component comprises after depositing a circuit layer 4 and 7 over a preformed substrate 5 and 55, joining a preformed die 1 and the preformed substrate 5 and 55. *~ See Figs 1 and 2, line 61 col. 5 through line 4 col. 7, and issued claim 11 ~* However, Sakurai fails to teaches that a method for fabricating a circuit component comprises after joining the preformed die 1 and the preformed substrate 5 and 55, depositing the circuit layer 4 and 7 over the preformed substrate 5 and 55, as claimed in claim 281.

Sakurai teaches that the method comprises depositing a copper bump 6 or 66 covered by gold plating over the circuit layer 4 and 7. *~ See FIGS. 2 and 3, and col. 6, lines 33-44 ~* However, the copper bump 6 or 66 covered by gold plating taught by Sakurai can not be deemed as a gold bump, whose principal material is gold, as claimed in claim 281.

As a result, withdrawal of rejection under 35 U.S.C. 102(b) to Claim 281 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent claim 281 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 287-300 patently define over the prior art as well.

Section II

Reconsideration of Claim 281 rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (US6,004,867) is requested based on the following remarks.

In merit to meet requirement of patentability, Applicants have amended Claim 281 with the limitation that "after said joining said preformed die and said preformed substrate, depositing a circuit layer comprising a first portion over said preformed die and a second portion over said preformed substrate but not over said preformed die".

Applicants respectfully assert that the method claimed in claim 281 patentably distinguishes over the citations by Kim et al. (US6,004,867).

Kim et al. teach that a method for fabricating a circuit component comprises joining a preformed wafer 300 and a preformed substrate 320 and then separating the preformed wafer 300 into multiple dies 310 and separating the preformed substrate 320 into multiple portions. ~ *See Figs. 5C and 5E, lines 27-35 col. 5, and lines 45-53 col. 6* ~ However, Kim et al. fail to teach that the method comprises after the die 310 is preformed, that is, separated from a wafer, joining the die 310 and the preformed substrate 320, as claimed in Claim 281.

Kim et al. teach that the method comprises after providing a circuit layer 321 and 322 in the preformed substrate 320, joining the preformed wafer 300 and the preformed substrate 320. ~ *See Fig. 5C, line 27 col. 5 through line 4 col. 6* ~ However, Kim et al. fail to teach that the method comprises after joining a preformed die and a preformed substrate, depositing a circuit layer comprising a first portion over said preformed die and a second portion over said preformed substrate but not over said preformed die, as claimed in Claim 281.

As a result, withdrawal of rejection under 35 U.S.C. 102(b) to Claim 281 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent claim 281 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 287-300 patently define over the prior art as well.

Response to Claims 282 and 301-319

As currently amended, independent claim 282 is recited below:

282. A method for fabricating a circuit component, comprising:

joining a preformed die and a preformed substrate;

after said joining said preformed die and said preformed substrate, forming an insulating layer comprising a first portion over said preformed die and a second portion over said preformed substrate but not over said preformed die, wherein said insulating layer comprises a porous structure; and

after said forming said insulating layer, separating said preformed substrate into multiple portions.

Reconsideration of Claim 282 rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al. (US6,396,148) in view of Wojnarowski et al. (US5,576,517) is requested based on the following remarks.

Applicants respectfully assert that the method claimed in claim 282 patentably distinguishes over the citation by Eichelberger et al. (US6,396,148) in view of Wojnarowski et al. (US5,576,517).

Eichelberger et al. teach that a method for fabricating a circuit component comprising joining a preformed die 102 and a preformed substrate 101; after said joining said preformed die 102 and said preformed substrate 101, forming an insulating layer 106 comprising a first portion over said preformed die 102 and a second portion over said preformed substrate 101 but not over said preformed die 102; and after said forming said insulating layer 106, separating said preformed substrate 101 into multiple portions. *~ See Figs 1 and 3A-3G, and lines 46-49 col. 8 ~* However, Eichelberger et al. fail to teach said insulating layer 106 comprises a porous structure.

It is should be noted that Eichelberger et al.'s method is applied for forming multiple chip packages by said separating said preformed substrate 101 into multiple portions. Wojnarowski et al.'s method is applied for forming only one chip package because Wojnarowski et al. do not teach a preformed substrate 10 joined with a preformed die 14 can be separated.

Applicants respectfully disagree the Examiner's opinion that the rejection is established under Eichelberger et al.'s method in view of Wojnarowski et al.'s method, because Eichelberger et al. and Wojnarowski et al. are conceptualized based on different bases: Eichelberger et al.'s method is based on forming multiple chip packages, but Wojnarowski et al.'s method is based on forming only one chip package.

The Examiner considers that it would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that applying the low dielectric constant porous layer, as taught by Wojnarowski et al., to Eichelberger et al.'s structure device would have been beneficial because Wojnarowski et al.'s teachings help to provide a low dielectric constant insulating layer which can apply to form high frequency circuits and reduce the need for laser ablation of material situated over air bridge structures and other microwave structures and devices. ~ *See line 23 of page 4 through line 4 of page 5, in the last Office Action mailed Aug. 9, 2006* ~

Even though Wojnarowski et al.'s method may have the above-mentioned advantages, no one teaches the structure comprising a porous insulating layer comprising a first portion over a preformed die and a second portion over a preformed substrate but not over the preformed die can be used for forming multiple chip packages by separating a preformed substrate, but not only for forming only one chip package.

As a result, withdrawal of rejection under 35 U.S.C. 103(a) to Claim 282 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent claim 282 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 301-319 patently define over the prior art as well.

Response to Claims 283 and 320-334

As currently amended, independent claim 283 is recited below:

283. A method for fabricating a circuit component, comprising:

joining a preformed die and a preformed substrate;

after said joining said preformed die and said preformed substrate, depositing a circuit layer comprising a first portion over said preformed die and a second portion over said preformed substrate but not over said preformed die, wherein said depositing said circuit layer comprises electroplating, and wherein said circuit layer comprises a part of a passive device; and

after said depositing said circuit layer, separating said preformed substrate into multiple portions.

Reconsideration of Claim 283 rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al. (US6,396,148, hereinafter "Eich-148") in view of Eichelberger et al. (US6,159,767, hereinafter "Eich-767") is requested based on the following remarks.

Applicants respectfully assert that the method claimed in claim 283 patentably distinguishes over the citation by Eich-148 in view of Eich-767.

Eich-148 teach that a method for fabricating a circuit component comprising joining a preformed die 102 and a preformed substrate 101; after said joining said preformed die 102 and said preformed substrate 101, depositing a circuit layer 109 comprising a first portion over said preformed die 102 and a second portion over said

preformed substrate 101 but not over said preformed die 102; and after said depositing said circuit layer 109, separating said preformed substrate 101 into multiple portions. *~ See Figs 1 and 3A-3G and lines 46-49 col. 8 ~* However, Eich-148 fail to teach said circuit layer 109 comprises a part of a passive device.

The Examiner considers that "Eich-767 teach a passive device 220 can be deposited ove multiple dies 102 for mixed signals applications". *~ See lines 14-16 in page 5, in the last Office Action mailed Aug. 9, 2006 ~*

Applicants respectfully traverse the Examiner's opinion. Eich-767 teaches the reference number of "220" indicates a surface mount electronic component. *~ See Fig. 6 and lines 11-13 col. 12 ~* It is not suitable that the reference number 220 is recognized as a passive device for rejecting Claim 183 because the surface mount electronic component may be an active device or a passive device.

Even under Eich-148's method in view of Eich-767's method, the subject matter that "said circuit layer 109 comprises a part of a passive device" can not be come up with.

Furthermore, even under Eich-148's method in view of Eich-767's method, the subject matter that "depositing a circuit layer comprising a part of a passive device comprises electroplating" can not be come up with. As a result, withdrawal of rejection under 35 U.S.C. 103(a) to Claim 283 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent claim 283 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 320-334 patently define over the prior art as well.

Response to Claims 284 and 335-346

As currently amended, independent claim 284 is recited below:

284. A method for fabricating a circuit component, comprising:

joining a preformed die and a preformed substrate, wherein said preformed die has a top surface at a horizontal level;

after said joining said preformed die and said preformed substrate, depositing a waveguide over said horizontal level; and

after said depositing said waveguide, separating said preformed substrate into multiple portions.

Reconsideration of Claim 284 rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al. (US6,396,148, hereinafter "Eich-148") in view of Eichelberger et al. (US6,159,767, hereinafter "Eich-767") is requested based on the following remarks.

Applicants respectfully assert that the method claimed in claim 284 patentably distinguishes over the citation by Eich-148 in view of Eich-767.

Eich-148 teach that a method for fabricating a circuit component comprising joining a preformed die 102 and a preformed substrate 101, wherein said preformed die 102 has a top surface at a horizontal level; and separating said preformed substrate 101 into multiple portions. ~ *See Figs 1 and 3A-3G and lines 46-49 col. 8* ~ However, Eich-148 fail to teach the subject matter that "after said joining said preformed die 102 and said preformed substrate 101, depositing a waveguide over said horizontal level, followed by said separating said preformed substrate 101 into multiple portions", as claimed in Claim 284.

The Examiner considers that "Eich-767 teach a passive device 220 can be deposited ove multiple dies 102 for mixed signals applications". ~ *See lines 14-16 in page 5, in the last Office Action mailed Aug. 9, 2006* ~

Applicants respectfully traverse the Examiner's opinion. Eich-767 teaches the

reference number of "220" indicates a surface mount electronic component. ~ *See Fig. 6 and lines 11-13 col. 12* ~ It is not suitable that the reference number 220 is recognized as a passive device or waveguide for rejecting Claim 184 because the surface mount electronic component may be an active device or a passive device, such as resistor, capacitor or inductor.

Even under Eich-148's method in view of Eich-767's method, the subject matter that "after joining a preformed die and a preformed substrate, depositing a waveguide over a horizontal level defined by a top surface of the preformed die, followed by separating the preformed substrate into multiple portions" can not be come up with. As a result, withdrawal of rejection under 35 U.S.C. 103(a) to Claim 284 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent claim 284 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 335-346 patently define over the prior art as well.

Response to Claims 285 and 347-358

As currently amended, independent claim 285 is recited below:

285. A method for fabricating a circuit component, comprising:

joining a preformed die and a preformed substrate, wherein said preformed die has a top surface at a horizontal level;

after said joining said preformed die and said preformed substrate, depositing a micro electronic mechanical element over said horizontal level; and

after said depositing said micro electronic mechanical element, separating said preformed substrate into multiple portions.

Reconsideration of Claim 285 rejected under 35 U.S.C. 102(e) as being

anticipated by Copeland (US6,439,728) is requested based on the following remarks.

Applicants respectfully assert that the method claimed in claim 285 patentably distinguishes over the citation by Copeland (US6,439,728).

Copeland teach that a method for fabricating a circuit component comprises depositing a micro electronic mechanical element 228 over a preformed die 220. ~ *See Fig. 4A, and lines 51-65 col. 4* ~ However, Copeland fails to teach that "after joining a preformed die and a preformed substrate, depositing the micro electronic mechanical element 228 over a horizontal level defined by a top surface of the preformed die, followed by separating the preformed substrate into multiple portions", as claimed in Claim 285.

As a result, withdrawal of rejection under 35 U.S.C. 103(a) to Claim 285 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent claim 285 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 347-358 patently define over the prior art as well.

Response to Claims 286 and 359-370

As currently amended, independent claim 286 is recited below:

286. A method for fabricating a circuit component, comprising:

joining a preformed die and a preformed substrate, wherein said preformed die has a top surface at a horizontal level;

after said joining said preformed die and said preformed substrate, depositing a filter over said horizontal level; and

after said depositing said filter, separating said preformed substrate into multiple portions.

Reconsideration of Claim 286 rejected under 35 U.S.C. 102(a) as being anticipated by Sekine et al. (US6,495,914) is requested based on the following remarks.

Applicants respectfully assert that the method claimed in claim 286 patentably distinguishes over the citations by Sekine et al. (US6,495,914).

Sekine et al. teach that a method for fabricating a circuitry component comprises joining a preformed die 47 and a preformed substrate 41, wherein said preformed die 47 has a top surface at a horizontal level; and separating said preformed substrate 41 into multiple portions. ~ *See Figs. 4a-4d, and lines 41-44 col. 6* ~ However, Sekine et al. fail to teach, hint or suggest after said joining said preformed die 47 and said preformed substrate 41, depositing a filter over said horizontal level, followed by said separating said preformed substrate 41 into multiple portions", as claimed in Claim 286.

As a result, withdrawal of rejection under 35 U.S.C. 103(a) to Claim 286 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent claim 286 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 359-370 patently define over the prior art as well.

CONCLUSION

Some or all of the pending claims are believed to be in condition for Allowance, and that is so requested. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

/Winston Hsu/ Date: 12/06/2006

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